REMARKS/ARGUMENTS

Claims 1-12 are pending in the application. The Applicants hereby request further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 2, the Examiner rejected claims 1-5 and 7-8 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Pub. No. 2002/0181633 ("Trans").

In paragraph 3, the Examiner stated that claim 6 would be allowable if rewritten in independent form.

In paragraph 4, the Examiner allowed claims 9-12.

For the following reasons, the Applicants submit that all of the pending claims are allowable over the cited references.

Claims 1-8

Claim 1 recites:

> 1. An apparatus for compensating for crosstalk in paths of a backplane, the apparatus comprising:
>
> a first adjuster, coupled to a first path, adapted to adjust a skew of a driver of the first path so as to compensate for crosstalk effects in the first path;
>
> a second adjuster, coupled to the first adjuster, adapted to generate an adjusted replica of the signal in the first path;
>
> a combiner, coupled to the second adjuster, adapted to combine the adjusted replica with a signal of a second path so as to compensate for crosstalk effects in the second path from the signal in the first path; and
>
> a clock synchronization generator adapted to generate a relatively low-speed clock signal,
>
> wherein the relatively low-speed clock signal aligns timing events of a relatively high-speed clock signal that coordinate events in the first and second paths.

In rejecting claim 1, the Examiner alleges that Trans discloses a second adjuster as element 208 in FIG. 3a (it appears that the Examiner actually intended to cite to element M208 in FIG. 5a, since there is no element 208 and no FIG. 3a in Trans). The Examiner further alleges that Trans discloses a combiner, citing to the element labeled (+) in FIG. 5e.

Claim 1 of the present application recites that the combiner is "coupled to the second adjuster" and "adapted to combine the adjusted replica with a signal of a second path so as to compensate for crosstalk effects in the second path from the signal in the first path."

Trans does not teach, disclose, or even suggest such a configuration. In paragraph [0024], Trans states that "FIG. 5a is the Time Sync Subsystem's Mode 2 Software Logic Block Diagram of the ITSync System. It is used to illustrate the software logics of the mode 2 component of the Subsystem's software major components, interfaces and applications." In paragraph [0028], Trans states that "FIG. 5e is the High Level Data Signal Detection Subsystem Block Diagram for the Com2000™ Signal Detection subsystem. It is used to illustrate the Signal Detection Circuit's major components, interfaces and

applications." Accordingly, element M208 of FIG. 5a is a software process shown in a software clock logic block diagram of a portion of Trans's ITSync Subsystem, and the element marked (+) in FIG. 5e is a combiner in the High Level Data Signal Detection Subsystem. Element M208 in FIG. 5a and the element marked (+) in FIG. 5e are in completely different parts of the system disclosed in Trans – one is in the ITSync Subsystem, and the other is in the High Level Data Signal Detection Subsystem. Thus, not only are these elements not coupled to one another, these elements are not even in the same circuit!

For this reason, Trans cannot possibly disclose a "combiner coupled to the second adjuster," as recited in claim 1. Moreover, for the same reason, Trans also cannot possibly disclose that the combiner is "adapted to combine the adjusted replica with a signal of a second path so as to compensate for crosstalk effects in the second path from the signal in the first path." The combiner in FIG. 5e has no relationship whatsoever to a first path and a second path – neither of which is shown in FIG. 5e – nor to any other path relating to element M208, if element M208 is to be considered the "second adjuster." In fact, other than the brief sentence in paragraph [0028] of the Brief Description of the Drawings in Trans referring to FIG. 5e generally, FIG. 5e is nowhere described or even mentioned anywhere in the specification of Trans!

Since Trans does not teach, disclose, or even suggest that the combiner is "coupled to the second adjuster" and "adapted to combine the adjusted replica with a signal of a second path so as to compensate for crosstalk effects in the second path from the signal in the first path," Trans cannot possibly anticipate claim 1.

Additionally, claim 1 recites "a clock synchronization generator adapted to generate a relatively low-speed clock signal," where "the relatively low-speed clock signal aligns timing events of a relatively high-speed clock signal that coordinate events in the first and second paths." Nowhere is this feature taught, disclosed, or even suggested in Trans. The Examiner cites to box 12 in FIG. 8-1 of Trans, labeled "Oscillator reference clock generator," as disclosing this feature. While box 12 is a reference clock generator, there is no disclosure, teaching, or suggestion any where in Trans of box 12 generating "a relatively low-speed clock signal" that "aligns timing events of a relatively high-speed clock signal that coordinate events in the first and second paths." Indeed, box 12 is mentioned only in paragraph [0122], which states that "[t]he Reference Clocks & Measurements Subsystem, shown in FIG. 8, includes the Disciplined Signal Generator (11), Oscillator Reference Clock Generator (12), Precision Reference Clock Generator (13). Measurement Source Selector (14), Measurement Reference Clock Generator (141), Corrected Output Generator (15) and The Precision Sampling Logic (16)." No further mention is made of box 12 at all, let alone the involvement of box 12 in the generation of "a relatively low-speed clock signal" that "aligns timing events of a relatively high-speed clock signal that coordinate events in the first and second paths." Since Trans fails to disclose these features, Trans cannot possibly anticipate claim 1.

For all these reasons, the Applicants submit that claim 1 is allowable over Trans. Since claims 2-5, 7, and 8 depend variously from claim 1, it is further submitted that those claims are also allowable over the cited references. The Applicants submit therefore that the rejections of claims under Section 102(b) have been overcome.

Claim 2

Claim 2 recites, *inter alia*, "a third adjuster, coupled to an adjacent channel and the combiner, adapted to generate an adjusted replica of a signal in the adjacent channel," and that "the combiner is further adapted to combine the adjusted replica of the signal of the adjacent channel with the signal of the second path so as to compensate for the crosstalk effects in the second path from the signal of the adjacent channel." In arguing that Trans anticipates claim 2, the Examiner alleges that the "third adjuster" is

element M210 of FIG. 3a (it appears that the Examiner actually intended to cite to element M210 in FIG. 5a, since there is no FIG. 3a in Trans).

Element M210 of FIG. 5a is a software process shown in a software clock logic block diagram of a portion of Trans's ITSync Subsystem, and the element marked (+) in FIG. 5e is a combiner in the High Level Data Signal Detection Subsystem. Element M210 in FIG. 5a and the element marked (+) in FIG. 5e are in completely different parts of the system disclosed in Trans – one is in the ITSync Subsystem, and the other is in the High Level Data Signal Detection Subsystem. Thus, not only are these elements not coupled to one another, these elements are not even in the same circuit!

Just as fully discussed above with reference to claim 1, the element marked (+) in FIG. 5e, which the Examiner cites as "a combiner," has no relationship whatsoever to a first path and a second path – neither of which is shown in FIG. 5e – nor to any other path relating to element M210, if element M210 is to be considered the "third adjuster." In fact, as mentioned above, other than the brief sentence in paragraph [0028] of the Brief Description of the Drawings in Trans referring to FIG. 5e generally, FIG. 5e is nowhere described or even mentioned anywhere in the specification of Trans!

For this reason, Trans cannot possibly disclose a "combiner coupled to the second adjuster," as recited in claim 1. Moreover, for the same reason, Trans also cannot possibly disclose that the combiner is "adapted to combine the adjusted replica of the signal of the adjacent channel with the signal of the second path so as to compensate for the crosstalk effects in the second path from the signal of the adjacent channel." The foregoing discussion provides additional reasons for the allowability of claim 2 over Trans.

Claim 3

Claim 3 recites, *inter alia*, that "the signal of the first path is a differential signal, the driver is a differential driver, and the first adjuster is adapted to adjust the positive-to-negative skew of the differential driver." In arguing that Trans anticipates claim 3, the Examiner cites, once again, only to the element marked (+) in FIG. 5e, without any explanation of how this element anticipates "the signal of the first path" being "a differential signal," the driver being "a differential driver, and the first adjuster being "adapted to adjust the positive-to-negative skew of the differential driver." There is no mention anywhere in the specification of Trans of the signal of the first path being "a differential signal." There is also no mention anywhere in the specification of Trans that a driver whose skew is being adjusted (per claim 1) is a "differential driver." Nor is there any disclosure of the first adjuster (element M203, according to the Examiner) being adapted "to adjust the positive-to-negative skew of the differential driver." The foregoing discussion provides additional reasons for the allowability of claim 3 over Trans.

Claim 4

Claim 4 recites, *inter alia*, that "the signal of the second path is a differential signal, and the combiner is a differential subtraction circuit." In arguing that Trans anticipates claim 4, the Examiner cites, once again, only to the element marked (+) in FIG. 5e, without any explanation of how this element anticipates "the signal of the second path" being "a differential signal," and the combiner being "a differential subtraction circuit." There is no mention anywhere in the specification of Trans of the signal of the second path being "a differential signal." There is no description provided at all for the element marked (+), let alone a description that this element is a differential subtraction circuit. The foregoing discussion provides additional reasons for the allowability of claim 4 over Trans.

Claim 5

Claim 5 recites, *inter alia*, "a phase-locked loop (PLL) adapted to generate a high-speed clock signal and a sync signal based on the high speed clock," and "at least one divider, each divider adapted to divide the high-speed clock signal into the low-speed clock signal, and wherein each divider is synchronized to each other divider based on the sync signal." The Examiner cites to paragraph [0123] of Trans as disclosing these features. Paragraph [0123] reads: "[0123] The Precision Sampling Logic (16) controls all aspects of the Precision measurement and timing functions. This includes signal clock tracking and management of the Precision signal processing, Phase Estimator Control of the measurements for timing solutions, phase/frequency transfer, security signature processing and PLL controls." Nowhere does this paragraph disclose anything about dividers, or dividing a high-speed clock signal into a low-speed clock signal, nor of a plurality of dividers synchronized to one another based on a sync signal. This paragraph does not even mention box 12, which the Examiner previously cited as being the "clock synchronization generator." The foregoing discussion provides additional reasons for the allowability of claim 5 over Trans.

Claim 6

Claim 6 has been indicated as allowable.

Claims 9-12

Claims 9-12 have been allowed.

In view of the above amendments and remarks, the Applicants believe that the now-pending claims are in condition for allowance. Therefore, the Applicants believe that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Fees

During the pendency of this application, the Commissioner for Patents is hereby authorized to charge payment of any filing fees for presentation of extra claims under 37 CFR 1.16 and any patent application processing fees under 37 CFR 1.17 or credit any overpayment to Mendelsohn & Associates, P.C. Deposit Account No. 50-0782.

The Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Respectfully submitted,

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